CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (original) A method for debugging a configuration process of a programmable logic device comprising:

initiating the configuration process for the programmable logic device;

capturing configuration process signals in the programmable logic device;

transferring the captured configuration process signals to a configuration analyzer; and

analyzing the transferred configuration process signals using the configuration analyzer.

2. (original) The method of claim 1 further comprising programming a configuration device coupled to the programmable logic device with a configuration bitstream.

3. (original) The method of claim 2 wherein initiating the configuration process comprises causing the programmable logic device to send normal configuration process signals to the configuration device, thereby causing the configuration device to provide the configuration bitstream.

4. (original) The method of claim 1 wherein initiating the configuration process comprises accessing the programmable logic device through a JTAG interface.

5. (original) The method of claim 4 further comprising:

executing a SAMPLE/PRELOAD instruction on the programmable logic device; and

executing an EXTEST instruction on the programmable logic device.

6. (original) The method of claim 5 further comprising executing a BYPASS instruction on a configuration device coupled to the programmable logic device.

7. (original) The method of claim 1 wherein analyzing the transferred configuration process signals comprises comparing the transferred configuration process signals with expected configuration process signals.

8. (original) The method of claim 7 wherein if the transferred configuration process signals and the expected configuration process signals do not match, then correcting the configuration process.

9. (currently amended) A system comprising:

a programmable logic device;

a configuration device coupled to the programmable logic device for providing a configuration bitstream to the programmable logic device; and

a configuration analyzer coupled to the programmable logic device for controlling the I/O pins of the programmable logic device, and analyzing configuration process signals received at the programmable logic device;

wherein the programmable logic device, the configuration device, and the analyzer form at least part of a JTAG chain.

10. (original) The system of claim 9 wherein the configuration device is a nonvolatile memory.

11. (original) The system of claim 9 wherein the programmable logic device is a field programmable gate array.

12. (original) The system of claim 9 wherein the programmable logic device comprises a boundary scan register.

13. (canceled).

14. (original) The system of claim 9 wherein the analyzer comprises a computer running a program for analyzing the configuration data.

15. (original) The system of claim 14 wherein the analyzer comprises a database of known configuration problems.

16. (original) A machine readable storage having stored thereon, a computer program having a plurality of code sections for debugging a configuration process of a programmable logic device, the code sections executable by a machine for causing the machine to perform the steps of:

initiating the configuration process for the programmable logic device;

capturing configuration process signals in the programmable logic device;

transferring the captured configuration process signals to a configuration analyzer; and

analyzing the transferred configuration process signals using the configuration analyzer.

17. (original) A configuration analyzer for debugging a configuration process of a programmable logic device comprising:

means for stepping through the configuration process;

means for capturing configuration process signals received by the programmable logic device at each step; and

means for comparing the captured configuration process signals with expected configuration process signals.